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Inventor Name Search Result

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Application#	Patent#	PG Pub#	Status	Date Filed	Title	Examiner Name
08511146	6147996		150	08/04/1995	PIPELINED MULTIPLE ISSUE PACKET SWITCH	NGO,RICKY
09001270	6424649		150	12/31/1997	SYNCHRONOUS PIPELINED SWITCH USING SERIAL TRANSMISSION	JUNG,MIN
09503552	6977930		150	02/14/2000	PIPELINED PACKET SWITCHING AND QUEUEING ARCHITECTURE	HARPER,KEVIN
09503976	6778546		150	02/14/2000	HIGH-SPEED HARDWARE IMPLEMENTATION OF MDRR ALGORITHM OVER A LARGE NUMBER OF QUEUES	TRAN,THIEN
09503988	6731644		150	02/14/2000	FLEXIBLE DMA ENGINE FOR PACKET HEADER MODIFICATION	TRAN,THIEN
09504479	6813243		150	02/14/2000	HIGH-SPEED HARDWARE IMPLEMENTATION OF RED CONGESTION CONTROL ALGORITHM	GEORGE,KEITH
09505934	6721316		150	02/14/2000	FLEXIBLE ENGINE AND DATA STRUCTURE FOR PACKET HEADER PROCESSING	GEORGE,KEITH
09549875	6831923		150	04/17/2000	PIPELINED	HO,CHUONG

					MULTIPLE ISSUE PACKET SWITCH	
10176819	7286525		150	06/21/2002	SYNCHRONOUS PIPELINED SWITCH USING SERIAL TRANSMISSION	JUNG,MIN
10219460	6980552		150	08/15/2002	PIPELINED PACKET SWITCHING AND QUEUEING ARCHITECTURE	HARPER,KEVIN
10227119	7304999	20040037322	150	08/24/2002	METHODS AND APPARATUS FOR PROCESSING PACKETS INCLUDING DISTRIBUTING PACKETS ACROSS MULTIPLE PACKET PROCESSING ENGINES AND GATHERING THE PROCESSED PACKETS FROM THE PROCESSING ENGINES	PHAM,BRENDA
10840126	Not Issued	20050249220	71	05/05/2004	Hierarchical QoS behavioral model	AHMED,SALMAN
10976299	7554907		150	10/27/2004	HIGH-SPEED HARDWARE IMPLEMENTATION OF RED CONGESTION CONTROL ALGORITHM	LEE,CHI HO
11242453	Not Issued	20060039374	93	10/03/2005	PIPELINED PACKET SWITCHING AND QUEUEING ARCHITECTURE	HARPER,KEVIN
11263473	Not Issued	20060050690	61	10/31/2005	Pipelined packet switching and queueing architecture	HARPER,KEVIN
12058783	Not Issued		30	03/31/2008	PROGRAMMABLE MATRIX PROCESSOR	BULLOCK JR,LEWIS
12395737	Not Issued		25	03/02/2009	OPTICAL PROGRAMMABLE MATRIX PROCESSOR	,

60908703	Not Issued		159	03/29/2007	PROGRAMMABLE MATRIX PROCESSOR	.
61032100	Not Issued		159	02/28/2008	OPTICAL PROGRAMMABLE MATRIX PROCESSOR	.

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